**CPHE 222: Organization, Architecture, and Assembly Language**

**Homework -- Chapter 5B**

**Exercise 1**: Answer the following questions for a 32 KB, two-way set associative cache with a block size of 2 KB.

1. How many bits are needed for the block offset? \_\_\_\_11\_\_\_\_
2. How many rows are there in this cache? \_\_\_\_8 \_\_\_\_
3. How many bits are needed for the cache index? \_\_\_\_\_3\_\_\_\_

**Exercise 2**: Answer the following questions for a 32 KB, eight-way set associative cache with a block size of 256 B.

1. How many bits are needed for the block offset? \_\_\_\_\_8\_\_\_\_
2. How many rows are there in this cache? \_\_\_\_\_4\_\_\_\_
3. How many bits are needed for the cache index? \_\_\_\_\_2\_\_\_\_

**Exercise 3**: Complete the two-way set associative cache diagram below to show its contents at the completion of the following sequence of memory accesses. Assume a write-back, write-allocate scheme with round robin replacement. Also, indicate where each access is a hit, miss, or miss with replace. Assume the block size is 256 bytes and leave the *Data* field blank.

|  |  |  |
| --- | --- | --- |
| **Byte address** | **Type** | **Hit or Miss?** |
| 0x19CD | LW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x0323 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x3145 | SW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x6363 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x03F4 | SW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x1914 | LW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |
| 0x83A1 | SW | ❑ Hit ❑ Miss ❑ Miss w/ Write Back |

**Two-Way Set Associative Cache**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **V** | **D** | **Tag** | **Data** | **V** | **D** | **Tag** | **Data** |
| 00: | 0 |  | 000110 | 0 |  |  |  | 0 |
| 01: | 1 | 0 | 001100 |  | 1 |  | 000110 | 0 |
| 10: |  |  |  | 1 |  |  |  | 0 |
| 11: | 1 | 1 | 000011 | 0 | 1 |  | 100000 | 0 |